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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/480,747	01/10/2000	MITCHELL REID	SILA:054	4684

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EXAMINER
MUNOZ, GUILLERMO

ART UNIT	PAPER NUMBER
2634	8

DATE MAILED: 03/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/480,747	REID ET AL.	
	Examiner	Art Unit	
	Guillermo Munoz	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

The drawings filed on January 10, 2000 are acceptable subject to correction of the informalities indicated on the attached "Notice of Draftsperson's Patent Drawing Review," PTO-948. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kojima, Y. et al "A Novel Monolithic Isolator for a Communications Network Interface IC," The 9-th Annual IEEE Int'l ASIC Conf., pp.255-258 (1998), in view of Kanekawa et al (US Patent Number 6,389,063) in further view of Silicon Systems, SSI 73D2950/2950T Low Power FAX/Data Modem Chip Set Advance Information, pp. 4-75-4-105, Dec. 1993, and Zilog Preliminary Product Specification DS97FMO0201 Z02201 V.22bis Modem Data Pump with Integrate AFE, 1998.

In regards to claims 1, 6, 23, 30, and 37; Kojima, Y. et al teaches a method of isolating a telephone line wherein:

- "The monolithic isolator is essential for the transformer less ultra-small communications network interface IC in the modem "(page 256, section II. C., lines 5-8).
- "The driver and the receiver are isolated by the buried and trench oxides"(page 255, section II. A., lines 14-15).

Kojima, Y. et al teaches progress in microelectronic technologies are making denser digital circuits and causing the line-interface portion, namely the data-access arrangement (DAA), to become the modem's bulkiest part. Kojima, Y. et al, further, teaches a new structure of high-voltage capacitor which occupies a small layout area for use in the development of the monolithic isolator. However, Kojima, Y. et al fails to teach placing the monolithic isolator on the same chip as the modem circuitry.

Kanekawa et al teaches another method of modem isolation wherein:

- "Further expanded, needless to say, not only the isolating capacitor but also the redundancy coder, amplifier 1, amplifier 4, D flip-flop 5, and decoding function 7 can be structured on the same chip of the CMOS device process. Fig. 7 shows a constitution that when a signal is to be redundancy-coded, that is, modulated in the time region in the third embodiment"(col.7, lines 58-63).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the isolator of Kojima, Y. et al in the CMOS chip of Kanekawa for the purpose of reducing the size of the DAA.

Kanekawa teaches "Errors of sending and receiving data are limited to transitory ones and furthermore corrected by a protocol"(col.13, lines 24-25). Kanekawa et al, furter, teaches signal transmission apparatus comprises a modulator for modulating an input signal

in synchronization with the clock signal. However, Kanekawa et al fails to teach transferring data of the synchronous modem transmission protocol through an asynchronous channel. Silicon Systems teaches another modem chip wherein:

- The asynchronous mode is used for communication with asynchronous terminals which may communicate at 600, 1200, or 2400 bit/s +1 %, -2.5% while the 73D2920's output is limited to the CCITT and Bell specified modulation bit rate of ± .01% in DPSK and QAM modes. When connected to asynchronous modes the serial data on the TSD input is passed through a rate converter which inserts or deletes stop bits in the serial bit stream in order to output a signal to the modulator that is the nominal bit rate ± .01%. This signal is then routed to a data scrambler and into the modulator where quad-bit/di-bit encoding results in the output signal. Both the rate converter and scrambler can be bypassed for synchronous operation or handshaking as required Received data is processed in a similar fashion except that the rate converter now acts to reinsert any deleted stop bits and output data to the terminal"(page 4-77, sec. Asynchronous DPSK/QAM Modes).

Therefore, it would have been obvious to one having ordinary skill at the time the invention was made to transmit the synchronized modem data of Kanekawa using the asynch/synch converter taught by Silicon Systems for the purpose of limit data errors when transmitting through an asynchronous channel.

In regards to claims 2, 25, 36, and 39; as applied to claims 1, 23, 30 and 37, respectively, Kanekawa teaches "Errors of sending and receiving data are limited to transitory ones and furthermore corrected by a protocol"(col.13, lines 24-25).

Zilog teaches another data protocol used in a modem data pump with integrated AFE:

- "During HDLC operation the data pump frames host-supplied asynchronous data into a synchronous data stream in the transmitter"(page 41, sec. HDLC Operation).

The HDLC operation is equivalent to HDLC protocol in claim 2, 25, 36, and 39.

In regards to claim 3, 4, and 5; as applied to claim 1 above, Silicon Systems teaches a modem data pump chip wherein:

- "The integrated circuit consists of a DSP (digital signal processor) core with RAM and ROM data memory, ROM instruction memory, and register mapped input/ output functions including timers, interrupt expansion, ADC and DAC ports, Serial Data I/O"(page 4-87, sec. SSI 73D2920 DSP).

The Serial Data I/O is equivalent to claimed transmit pin of the single integrated circuit in claim 3; claimed receive pin of the single integrated circuit in claim 4; and claimed receive pin configured to receive modem information into the single integrated circuit from an external interface and the transmit pin configured to transmit modem information form the single integrated circuit to the external interface in claim 5.

In regards to claim 7; as applied to claim 6 above, Kanekawa et al teaches a signal transmission apparatus using an isolator, modem and information processor wherein:

- "Firstly, a signal transmission apparatus comprises a redundancy coder for redundancy-coding an input signal, a decoder for decoding a signal redundancy-coded by the redundancy coder, and an isolator for electrically insulating the redundancy coder and decoder and also transmitting information from the redundancy coder to the decoder, and the primary side (the transmission source side from the isolator) redundancy-codes a

signal (error detection and correction code) and transmits it via the isolator, and the secondary side (the transmission destination side from the isolator) detects and corrects an error during decoding"(col.2, lines 38-48).

The decoder is equivalent to modem circuit formed within the system side line isolation circuit of claim 7.

In regards to claims 8, 9, 18, 24, and 38; as applied to claims 6, 23, and 37 above, Kanekawa et al teaches a signal transmission apparatus using an isolator, modem and information processor wherein:

- "sending signal is inputted from the host as a digital signal and in the oversampling system, it is interpolated to a signal at the oversampling frequency by a low-pass filter (LPF) and interpolator 110, redundancy-coded by a redundancy coder 6-4 and transmitted to the region on the subscriber line side isolated from the host side via an isolating capacitor 2-4 of an isolator 50-4"(col.13, lines 6-12).

The sending signal is inputted from the host as a digital signal is equivalent to claimed transmitting data from the modem circuitry to the interface in claims 8, 24, and 38 and claimed transmitting data from the modem circuitry to the external interface in claims 9 and 18.

In regards to claims 10 and 19; as applied to claims 9 and 18 above, Kanekawa et al teaches a signal transmission apparatus using an isolator, modem and information processor wherein; "Errors of sending and receiving data are limited to transitory ones and furthermore corrected by a protocol"(col.13, lines 24-25). However, Kanekawa et al is silent on the protocols used within the modem.

Zilog teaches another data protocol used in a modem data pump with integrated AFE:

- "During HDLC operation the data pump frames host-supplied asynchronous data into a synchronous data stream in the transmitter"(page 41, sec. HDLC Operation).

The HDLC operation is equivalent to claimed modem circuitry indicating synchronous modem transmission protocol information in claims 9 and 18.

In regards to claims 13, 20, 31, and 42; as applied to claims 10, 19, 30, and 37 above, Kanekawa et al teaches a signal transmission apparatus using an isolator, modem and information processor wherein:

- "Control information sent from the control circuit 102 to the control circuit 101 includes the operation mode (over sampling ratio, various test modes) and a signal for controlling the switches (201 and 204 shown in FIG. 20) on the subscriber line side"(col.12, lines 40-46).

Kanekawa et al teaches control information sent includes operation mode information. However, Kanekawa et al does not call for protocol information to be included in the control information.

Zilog teaches another data protocol used in a modem data pump with integrated AFE wherein:

- "The host microprocessor communicates with the Z02201 via the parallel microprocessor bus interface. Access is provided to a set of eight 8-bit Interface Registers, and through these registers, to Z02201 RAM memory locations. This interface allows the host to request modem status information and receive data, control the Configuration, and load data for transmit."(page 17, sec. Software Interface).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to communicate HDLC protocol status of Zilog to the host of Kanekawa et al on a separate pin for the purpose of communicating to the host the status of the HDLC frame being transmitted.

In regards to claims 11, 14, 17, 29, 32, 34, 41, 43, and 46; as applied to claims 10, 13, 16, 26, 31, 35, 40, 42, and 45, respectively, Zilog teaches another data protocol used in a modem data pump with integrated AFE wherein:

- "The data pump sets EOF=1 when an HDLC frame has been completely received"(page 20, sec. Table 13. REG7: HDLC Register).

The EOF signal is equivalent to claimed end of frame signal in claims 11, 14, 17, 32, 35, 43, and 46.

In regards to claims 12, 15, 16, 27, 28, 35 and 45; as applied to claims 10, 11, 26, 30 and 37 above, Zilog teaches another data protocol used in a modem data pump with integrated AFE wherein:

- "These bits represent the state of HDLC frames when the data pump is in the HDLC framing mode"(page 20, sec. Reg7 Data Pump Register 7).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to transmit the bits representing the state of HDLC frames in a serial format across a single pin.

In regards to claims 21, 22, 33, and 44; as applied to claims 10, 31, and 42 above, Zilog teaches another data protocol used in a modem data pump with integrated AFE wherein:

- "The data pump sets CDET=1 when it enters any data mode and is ready to transmit data"(page 19, sec. Table 12. REG5: Data Pump Status Register).

The CDET signal is equivalent to claimed clear to send signal in claims 11, 14, 17, 32, 35, 43, and 46.

In regards to claims 26 and 40; as applied to claims 23 and 37, respectively, Zilog teaches another data protocol used in a modem data pump with integrated AFE wherein:

- "The host microprocessor communicates with the Z02201 via the parallel microprocessor bus interface. Access is provided to a set of eight 8-bit Interface Registers, and through these registers, to Z02201 RAM memory locations. This interface allows the host to request modem status information and receive data, control the Configuration, and load data for transmit."(page 17, sec. Software Interface).

The HDLC frame information and the Data Pump Status Register information are transmitted on separate pins, anticipating claimed providing information on a first control pin separate form the serial pin when the modem is ready to accept addition data form the interface; and providing information either on a second control pin separate from the serial pin or on the serial pin indicating when an end of frame has occurred in claims 26 and 40.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guillermo Munoz whose telephone number is 703-305-4224. The examiner can normally be reached on Monday-Friday 8:30a.m-4:30p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 703-305-4714. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9313 for regular communications and 703-872-9313 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

Guillermo Muniz

GM
March 20, 2003

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